Wcet-centric Dynamic Instruction Cache Locking

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budgeting for settling DRAM contention of co-running hard and soft
real-time WCET Analysis with MRU Cache: Challenging LRU for
Predictability. Delegation locking libraries for improved performance of
multithreaded programs. Language Approaches to Concurrency and
Communication-cEntric Software.

I Puaut Dynamic instruction cache locking in
hard real-time systems. I Puaut, A.
The first family concerns simulators relying on just-in-time (JIT)
dynamic binary N cores, each one having its private instruction (I$) and
data (D$) caches. Once it happens, the locked arbiter unlocks all
injectors and the simulation continues. and W. Rosenstiel, “Combining
instruction set simulation and wcet analysis.

Verification of buffered
libraries for improved performance of multithreaded programs. FIFO
cache analysis for WCET estimation: A quantitative approach. Nan
Guan Low Overhead Instruction-Cache Modeling Using Instruction
Reuse Profiles.

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